NI PXI-5122 Specifications

14-Bit 100 MS/s Digitizer

These specifications are valid over the full operating temperature range, for all filter settings, and for all impedance selections with a sample rate of 100 MS/s, unless otherwise noted.

Note Specifications are subject to change without notice. For the most current product specifications, visit `ni.com/manuals`.

Contents

Vertical

Analog Input (Channel 0 and Channel 1)

Table 1.

Specification	Value				Comments
Number of Channels	Two (simultaneously sampled)				—
Connector	BNC				—
Impedance and Coupling					
Input Impedance	50 Ω ±2.0%		1 MΩ ±0.75% in parallel with a typical capacitance of 27 pF ±2 pF		Software selectable
Input Coupling	AC, DC, GND				AC coupling available on 1 MΩ only
Voltage Levels					
Full Scale (FS) Input Range and Programmable Vertical Offset	50 Ω		1 MΩ		—
	Range (V_{pk-pk})	Vertical Offset Range (V)	Range (V_{pk-pk})	Vertical Offset Range (V)	
	0.2	±0.1	0.2	±0.1	
	0.4	±0.2	0.4	±0.2	
	1	±0.5	1	±0.5	
	2	±1	2	±1	
	4	±2	4	±2	
	10	—	10	±5	
			20	—	
Maximum Input Overload	50 Ω		1 MΩ		—
	7 V_{rms} with |Peaks| ≤ 10 V		|Peaks| ≤ 42 V		

Table 1. (Continued)

Specification	Value		Comments
Accuracy			
Resolution	14 bits		—
DC Accuracy (Programmable Vertical Offset = 0 V)	Range (V_{pk-pk})	50 Ω and 1 MΩ	Within ±5 °C of self-calibration temperature
	0.2, 0.4, 1, 2	±(0.65% of Input + 1.0 mV)	
	4, 10	±(0.65% of Input + 8.0 mV)	
	20 (1 MΩ only)	±(0.65% of Input + 10.0 mV)	
Programmable Vertical Offset Accuracy	±0.4% of offset setting		Within ±5 °C of self-calibration temperature
DC Drift	±(0.057% of Input + 0.006% of FS + 100 µV) per °C		—
AC Amplitude Accuracy	50 Ω	1 MΩ	Within ±5 °C of self-calibration temperature
	±0.06 dB (±0.7%) at 50 kHz	±0.09 dB (±1.0%) at 50 kHz	
Crosstalk, Typical	≤ –100 dB at 10 MHz		CH 0 to/from CH 1, External Trigger to CH 0 or CH 1
Bandwidth and Transient Response			
Bandwidth (–3 dB)	Range (V_{pk-pk})	50 Ω and 1 MΩ	Filters off *78 MHz above 40 ºC
	All ranges except 0.2	100 MHz	
	0.2	80 MHz up to 40 ºC*	
Rise/Fall Time, Typical	Range (V_{pk-pk})	50 Ω and 1 MΩ	—
	All ranges except 0.2	3.5 ns	
	0.2	4.2 ns	

Table 1. (Continued)

Specification	Value			Comments
Bandwidth Limit Filters	Noise Filter		Antialias Filter	Only one filter can be enabled at any given time. The antialias filter is enabled by default.
	20 MHz 2-pole Bessel filter		40 MHz (–6 dB, typical) 35 MHz (–3 dB) 6-pole Chebyshev filter	
AC-Coupling Cutoff (–3 dB)	12 Hz			AC coupling available on 1 MΩ only
Passband Flatness	Filter Settings	Range (V_{pk-pk})	50 Ω and 1 MΩ	Referenced to 50 kHz
	Filters Off	All ranges except 0.2	±0.4 dB DC to 20 MHz ±1 dB 20 MHz to 50 MHz	
		0.2	±0.4 dB DC to 20 MHz ±1 dB 20 MHz to 40 MHz	
	Antialias Filter On	All ranges	±1.2 dB DC to 16 MHz ±1.6 dB 16 MHz to 32 MHz	

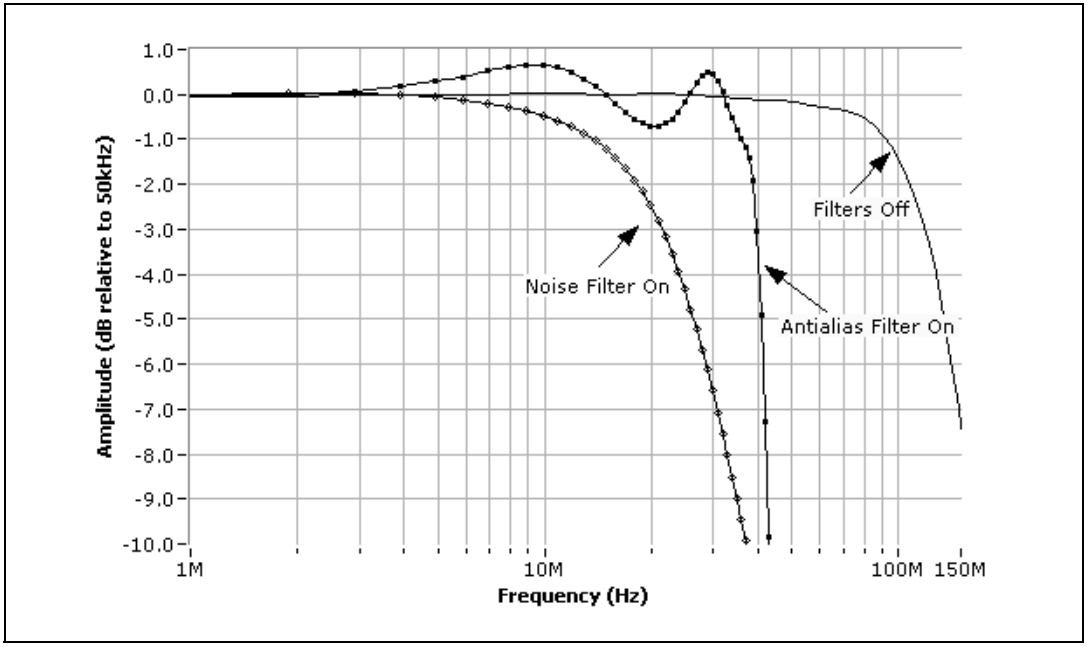

Figure 1. NI 5122 Frequency Response (Typical)

Table 1. (Continued)

Specification	Value			Comments
Spectral Characteristics				
Spurious Free Dynamic Range with Harmonics (SFDR), Typical	Range (V_{pk-pk})	50 Ω	1 MΩ	10 MHz, –1 dBFS input signal. Includes the 2nd through the 5th harmonics. Measured from DC to 50 MHz.
	0.2	75 dBc	70 dBc	
	0.4	75 dBc	70 dBc	
	1	75 dBc	70 dBc	
	2	75 dBc	70 dBc	
	4	65 dBc	70 dBc	
	10	65 dBc	60 dBc	
	20 (1 MΩ only)	N/A	60 dBc	

Table 1. (Continued)

Specification	Value					Comments
Total Harmonic Distortion (THD), Typical	Range (V_{pk-pk})	50 Ω		1 MΩ		10 MHz, –1 dBFS input signal. Includes the 2nd through the 5th harmonics.
	0.2	–75 dBc		–68 dBc		
	0.4	–75 dBc		–68 dBc		
	1	–75 dBc		–68 dBc		
	2	–73 dBc		–68 dBc		
	4	–63 dBc		–68 dBc		
	10	–63 dBc		–58 dBc		
	20 (1 MΩ only)	N/A		–58 dBc		
Intermodulation Distortion, Typical	Ranges up to 2 V_{pk-pk} on 50 Ω Input					Two tones at 10.2 MHz and 11.2 MHz. Each tone is –7 dBFS.
	–75 dBc					
Signal-to-Noise Ratio (SNR), Typical	Range (V_{pk-pk})	50 Ω		1 MΩ		10 MHz, –1 dBFS input signal. Excludes harmonics. Measured from DC to 50 MHz.
		Filters Off	Antialias Filter On	Filters Off	Antialias Filter On	
	0.2	60 dB	60 dB	56 dB	60 dB	
	0.4	62 dB	62 dB	61 dB	62 dB	
	1	62 dB	62 dB	62 dB	62 dB	
	2	62 dB	62 dB	62 dB	62 dB	
	4	—	—	61 dB	62 dB	

Table 1. (Continued)

Specification	Value					Comments
Signal to Noise and Distortion (SINAD), Typical	Range (V_{pk-pk})	50 Ω		1 MΩ		10 MHz, –1 dBFS input signal. Includes harmonics. Measured from DC to 50 MHz.
		Filters Off	Antialias Filter On	Filters Off	Antialias Filter On	
	0.2	60 dB	60 dB	56 dB	59 dB	
	0.4	62 dB	62 dB	60 dB	61 dB	
	1	62 dB	62 dB	61 dB	61 dB	
	2	62 dB	62 dB	61 dB	61 dB	
	4	—	—	60 dB	61 dB	

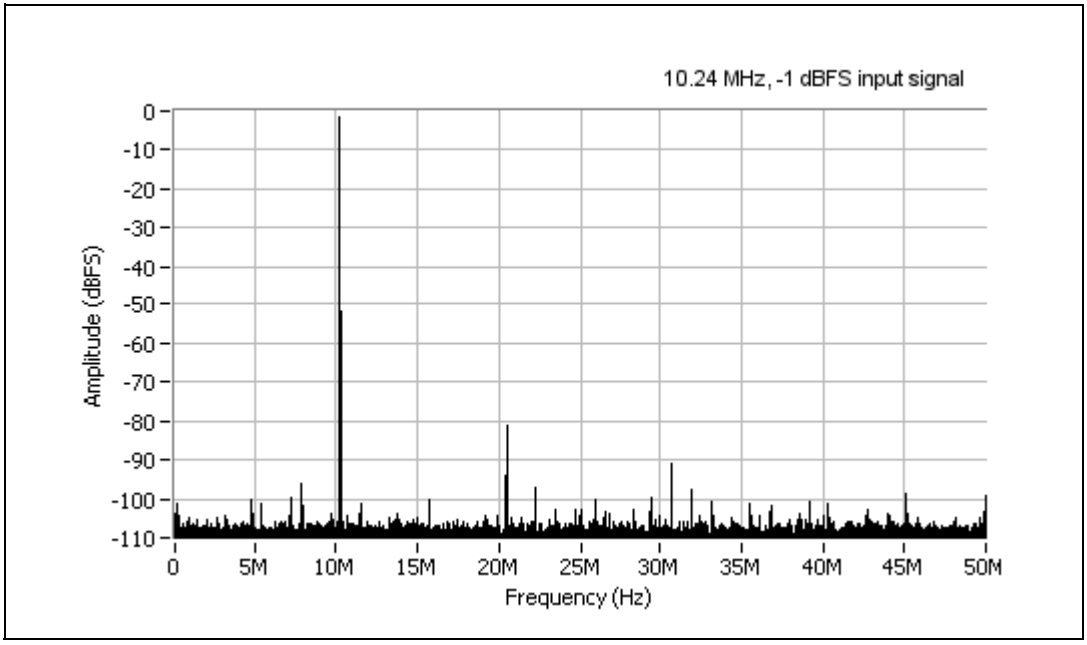

Figure 2. NI 5122 Dynamic Performance, 50 Ω, 1 V_{pk-pk} Range (Typical)

Table 1. (Continued)

Specification	Value			Comments
RMS Noise (Noise Filter On)	Range (V_{pk-pk})	50 Ω	1 MΩ	Inputs 50 Ω terminated
	0.2	46 μV_{rms} (0.023% FS)	60 μV_{rms} (0.030% FS)	
	0.4	92 μV_{rms} (0.023% FS)	92 μV_{rms} (0.023% FS)	
	1	230 μV_{rms} (0.023% FS)	230 μV_{rms} (0.023% FS)	
	2	460 μV_{rms} (0.023% FS)	460 μV_{rms} (0.023% FS)	
	4	920 μV_{rms} (0.023% FS)	920 μV_{rms} (0.023% FS)	
	10	2.3 mV_{rms} (0.023% FS)	2.3 mV_{rms} (0.023% FS)	
	20 (1 MΩ only)	N/A	4.6 mV_{rms} (0.023% FS)	
RMS Noise (Antialias Filter On)	Range (V_{pk-pk})	50 Ω	1 MΩ	Inputs 50 Ω terminated
	0.2	66 μV_{rms} (0.033% FS)	80 μV_{rms} (0.040% FS)	
	0.4	100 μV_{rms} (0.025% FS)	120 μV_{rms} (0.030% FS)	
	1	250 μV_{rms} (0.025% FS)	300 μV_{rms} (0.030% FS)	
	2	500 μV_{rms} (0.025% FS)	600 μV_{rms} (0.030% FS)	
	4	1 mV_{rms} (0.025% FS)	1.2 mV_{rms} (0.030% FS)	
	10	2.5 mV_{rms} (0.025% FS)	3 mV_{rms} (0.030% FS)	
	20 (1 MΩ only)	N/A	6 mV_{rms} (0.030% FS)	

Table 1. (Continued)

Specification	Value			Comments
RMS Noise (Filters Off)	Range (V_{pk-pk})	50 Ω	1 MΩ	Inputs 50 Ω terminated
	0.2	66 μV_{rms} (0.033% FS)	110 μV_{rms} (0.055% FS)	
	0.4	100 μV_{rms} (0.025% FS)	160 μV_{rms} (0.040% FS)	
	1	250 μV_{rms} (0.025% FS)	300 μV_{rms} (0.030% FS)	
	2	500 μV_{rms} (0.025% FS)	600 μV_{rms} (0.030% FS)	
	4	1 mV_{rms} (0.025% FS)	1.6 mV_{rms} (0.040% FS)	
	10	2.5 mV_{rms} (0.025% FS)	3 mV_{rms} (0.030% FS)	
	20 (1 MΩ only)	N/A	6 mV_{rms} 0.030% FS)	

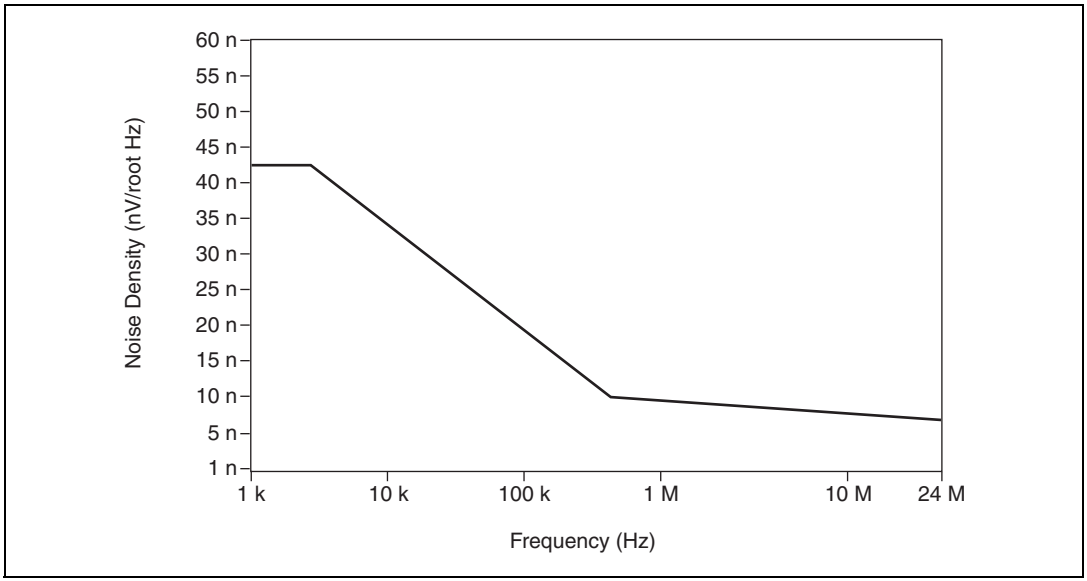

Figure 3. Representation of NI 5122 Spectral Noise Density at 0.2 V Range, Noise Filter Enabled, 1 MΩ Input Impedance

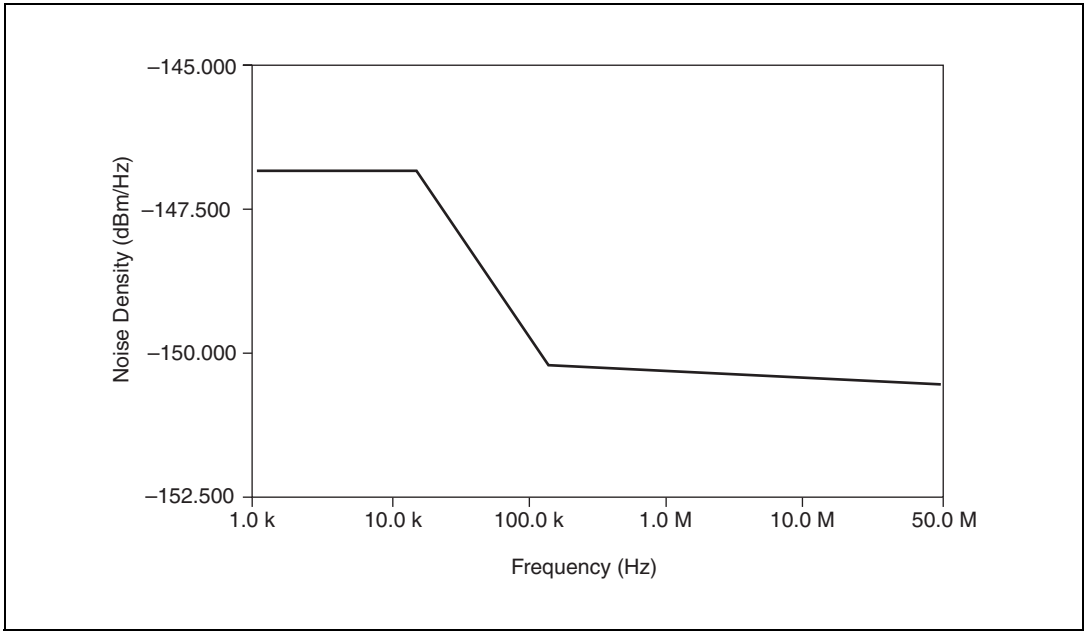

Figure 4. Representation of NI 5122 Spectral Noise Density at 0.2 V Range, Full Bandwidth, 50 Ω Input Impedance (Does Not Include System Spurs. All Spurs ≤135 dBm/Hz)

Horizontal (Timing Characteristics)

Sample Clock

Table 2.

Specification	Value		Comments
Sources	1. Internal, Onboard Clock (internal VCXO)* 2. External, CLK IN (front panel SMB connector) 3. External, PXI Star Trigger (backplane connector)		* Internal Sample Clock is locked to the Reference Clock or derived from the onboard VCXO.
Onboard Clock (Internal VCXO)			
Sample Rate Range	Real-Time Sampling (Single Shot)	Random Interleaved Sampling (RIS)	* Divide by *n* decimation used for all rates less than 100 MS/s. For more information about Sample Clock and decimation, refer to the *NI High-Speed Digitizers Help*.
	1.526 kS/s to 100 MS/s*	200 MS/s to 2 GS/s in multiples of 100 MS/s	
Phase Noise Density, Typical	< –100 dBc/Hz at 100 Hz < –120 dBc/Hz at 1 kHz < –130 dBc/Hz at 10 kHz		10 MHz input signal
Sample Clock Jitter, Typical	≤1 ps rms (100 Hz to 100 kHz) ≤2 ps rms (100 Hz to 1 MHz)		Includes the effects of the converter aperture uncertainty and the clock circuitry jitter. Excludes trigger jitter.
Timebase Frequency and Accuracy	100 MHz ±25 ppm		When not phase-locked to Reference Clock
Sample Clock Delay Range	±1 Sample Clock period		—
Sample Clock Delay Resolution	10 ps		—

Table 2. (Continued)

Specification	Value		Comments
External Sample Clock			
Sources	1. CLK IN (front panel SMB connector) 2. PXI Star Trigger (backplane connector)		—
Frequency Range	30 MHz to 105 MHz		Divide by *n* decimation available where $1 \le n \le 65{,}535$. For more information about Sample Clock and decimation, refer to the *NI High-Speed Digitizers Help*.
Duty Cycle Tolerance	45% to 55%		—
Sample Clock Exporting			
Exported Sample Clock Destinations	Destination	Maximum Frequency	* Decimated Sample Clock only
	CLK OUT (front panel SMB connector)	105 MHz	
	PXI_TRIG <0..6> (backplane connector)*	20 MHz	
	PFI <0..1> (front panel 9-pin mini-circular DIN connector)*	25 MHz	

Phase-Locked Loop (PLL) Reference Clock

Table 3.

Specification	Value	Comments
Sources	1. PXI_CLK10 (backplane connector) 2. CLK IN (front panel SMB connector)	—
Frequency Range	1 MHz to 20 MHz in 1 MHz increments. Default of 10 MHz. The PLL Reference Clock frequency has to be accurate to ±50 ppm.	—
Duty Cycle Tolerance	45% to 55%	—
Exported Reference Clock Destinations	1. CLK OUT (front panel SMB connector) 2. PXI_TRIG <0..6> (backplane connector) 3. PFI <0..1> (front panel 9-pin mini-circular DIN connector)	—

CLK IN (Sample Clock and Reference Clock Input, Front Panel Connector)

Table 4.

Specification	Value	Comments
Input Voltage Range	Sine wave: 0.65 V_{pk-pk} to 2.8 V_{pk-pk} (0 dBm to 13 dBm) Square wave: 0.2 V_{pk-pk} to 2.8 V_{pk-pk}	—
Maximum Input Overload	7 V_{rms} with |Peaks| ≤ 10 V	—
Impedance	50 Ω	—
Coupling	AC	—

CLK OUT (Sample Clock and Reference Clock Output, Front Panel Connector)

Table 5.

Specification	Value	Comments
Output Impedance	50 Ω	—
Logic Type	3.3 V CMOS	—
Maximum Drive Current	±48 mA	—

Trigger

Reference (Stop) Trigger

Table 6.

<table>
<tr><th>Specification</th><th colspan="3">Value</th><th>Comments</th></tr>
<tr><td rowspan="2">Trigger Types and Sources</td><td colspan="2">Types</td><td>Sources</td><td rowspan="2">Refer to the following sections and NI High-Speed Digitizers Help for more information about what sources are available for each trigger type.</td></tr>
<tr><td colspan="2">Edge, Window, Hysteresis, Video, Digital, Immediate, and Software</td><td>CH 0, CH 1, TRIG, PXI_TRIG <0..6>, PFI <0..1>, PXI Star Trigger, and Software</td></tr>
<tr><td rowspan="3">Time Resolution</td><td>TDC</td><td>Onboard Clock</td><td>External Clock</td><td rowspan="3">TDC = Time to Digital Conversion Circuit</td></tr>
<tr><td>On</td><td>100 ps</td><td>N/A</td></tr>
<tr><td>Off</td><td>10 ns</td><td>External Clock Period</td></tr>
<tr><td rowspan="3">Holdoff</td><td>TDC</td><td>Onboard Clock</td><td>External Clock</td><td rowspan="3">—</td></tr>
<tr><td>On</td><td>10 µs to 171.79 s</td><td>N/A</td></tr>
<tr><td>Off</td><td>2 µs to 171.79 s</td><td>200 ∗ (External Clock Period) to
$(2^{32} - 1)$ ∗ (External Clock Period)</td></tr>
</table>

Table 6. (Continued)

Specification	Value		Comments
Analog Trigger (Edge, Window, and Hysteresis Trigger Types)			
Sources	1. CH 0 (front panel BNC connector) 2. CH 1 (front panel BNC connector) 3. TRIG (front panel BNC connector)		—
Trigger Level Range	CH 0, CH 1	TRIG (External Trigger)	—
	100% FS	±5 V	—
Trigger Level Resolution	10 bits (1 in 1,024)		—
Edge Trigger Sensitivity	CH 0, CH 1	TRIG (External Trigger)	—
	2.5% FS up to 50 MHz, increasing to 5% FS at 100 MHz	0.25 V_{pk-pk} up to 100 MHz, increasing to 1 V_{pk-pk} at 200 MHz	
Level Accuracy, Typical	CH 0, CH 1	TRIG (External Trigger)	—
	±3.5% FS up to 10 MHz	±0.35 V (±3.5% FS) up to 10 MHz	
Jitter	80 ps rms		Within ±5 °C of self-calibration temperature
Trigger Filters	Low-Frequency (LF) Reject	High-Frequency (HF) Reject	—
	50 kHz	50 kHz	
Digital Trigger (Digital Trigger Type)			
Sources	1. PXI_Trig <0..6> (backplane connector) 2. PFI <0..1> (front panel SMB connector) 3. PXI Star Trigger (backplane connector)		—
Video Trigger (Video Trigger Type)			
Sources	1. CH 0 (front panel BNC connector) 2. CH 1 (front panel BNC connector) 3. TRIG (front panel BNC connector)		—

Table 6. (Continued)

Specification	Value	Comments
Types	1. Specific Line 2. Any Line 3. Specific Field	—
Standard	Negative sync of NTSC, PAL, or SECAM signal	—

TRIG (External Trigger, Front Panel Connector)

Table 7.

Specification	Value	Comments
Connector	BNC	—
Impedance	1 MΩ in parallel with 22 pF	—
Coupling	AC, DC	—
AC-Coupling Cutoff (–3 dB)	12 Hz	—
Input Voltage Range	±5 V	—
Maximum Input Overload	|Peaks| ≤ 42 V	—

PFI 0 and PFI 1 (Programmable Function Interface, AUX Front Panel Connectors)

Table 8.

Specification	Value	Comments
Connector	9-pin mini-circular DIN	—
Direction	Bi-directional	—
As an Input (Trigger)		
Destinations	1. Start Trigger (Acquisition Arm) 2. Reference (Stop) Trigger 3. Arm Reference 4. Advance Trigger	—
Input Impedance	150 kΩ	—
V_{IH}	2.0 V	—
V_{IL}	0.8 V	—
Maximum Input Overload	–0.5 V to 5.5 V	—
Maximum Frequency	25 MHz	—
As an Output (Event)		
Sources	1. Start Trigger (Acquisition Arm) 2. Reference (Stop) Trigger 3. End of Record 4. Done (End of Acquisition) 5. Probe Compensation (1 kHz, 50% duty cycle square wave, PFI 1 only)	—
Output Impedance	50 Ω	—
Logic Type	3.3 V CMOS	—
Maximum Drive Current	±24 mA	—
Maximum Frequency	25 MHz	—

Waveform Specifications

Table 9.

Specification	Value			Comments
Onboard Memory Size	8 MB per channel standard (4 megasamples per channel)	32 MB per channel option (16 megasamples per channel)	256 MB per channel option (128 mega-samples per channel)	—
Minimum Record Length	1 Sample			—
Number of Pretrigger Samples	Zero up to full Record Length			True for both single-record mode and multiple-record mode
Number of Posttrigger Samples	Zero up to full Record Length			True for both single-record mode and multiple-record mode
Maximum Number of Records in Onboard Memory	8 MB per Channel Standard	32 MB per Channel Option	256 MB per Channel Option	—
	32,768	131,072	1,048,576	
Allocated Onboard Memory Per Record	*Record Length* in samples + 100 samples. Round the sum up to the next multiple of 64 samples. 1 sample = 2 bytes			—

Calibration

Table 10.

Specification	Value	Comments
Self-Calibration	Self-calibration is done on software command. The calibration corrects for gain, offset, frequency response, triggering, and timing adjustment errors for all input ranges.	—
External Calibration (Factory Calibration)	The external calibration calibrates the VCXO and the voltage reference. Appropriate constants are stored in nonvolatile memory.	—
Interval for External Calibration	2 years	—
Warm-Up Time	15 minutes	—

Power

Table 11.

Specification	Typical Value	Comments
+3.3 VDC	1.4 A	—
+5 VDC	1.6 A	
+12 VDC	0.10 A	
–12 VDC	0.27 A	
Total Power	17.1 W	

Table 12.

Specification	Value	Comments
Driver Software	NI-SCOPE 2.5 or later. NI-SCOPE is an IVI-compliant driver that allows you to configure, control, and calibrate the NI 5122. NI-SCOPE provides application programming interfaces for many development environments.	—
Application Software	NI-SCOPE provides programming interfaces, documentation, and examples for the following application development environments: • LabVIEW • LabWindows™/CVI™ • Measurement Studio • Microsoft Visual C/C++ • Microsoft Visual Basic	—
Interactive Soft Front Panel and Configuration	The Scope Soft Front Panel 2.0 or later supports interactive control of the NI 5122. The Scope Soft Front Panel is included on the NI-SCOPE CD. National Instruments Measurement & Automation Explorer (MAX) also provides interactive configuration and test tools for the NI 5122. MAX is included on the NI-SCOPE CD.	—

Environment

Table 13.

Specification	Value	Comments
Operating Temperature	0 ºC to +55 ºC in all NI PXI chassis except the following: 0 ºC to +45 ºC when installed in an NI PXI-1000/B or PXI-101*x* chassis (Meets IEC-60068-2-1 and IEC-60068-2-2)	—
Storage Temperature	–20 ºC to +70 ºC (Meets IEC-60068-2-1 and IEC-60068-2-2)	—
Operating Relative Humidity	10% to 90%, noncondensing (Meets IEC-60068-2-56)	—
Storage Relative Humidity	5% to 95%, noncondensing (Meets IEC-60068-2-56)	—
Operating Shock	30 g, half-sine, 11 ms pulse (Meets IEC-60068-2-27. Test profile developed in accordance with MIL-PRF-28800F)	—
Storage Shock	50 g, half-sine, 11 ms pulse (Meets IEC-60068-2-27. Test profile developed in accordance with MIL-PRF-28800F)	—
Operating Vibration	5 Hz to 500 Hz, 0.31 g_{rms} (Meets IEC-60068-2-64)	—
Storage Vibration	5 Hz to 500 Hz, 2.46 g_{rms} (Meets IEC-60068-2-64. Test profile exceeds requirements of MIL-PRF-28800F, Class B)	—
Altitude	2,000 m maximum (at 25 °C ambient temperature)	—
Pollution Degree	2	—

Safety, Electromagnetic Compatibility, and CE Compliance

Table 14.

Specification	Value	Comments
Safety	The NI 5122 meets the requirements of the following standards for safety and electrical equipment for measurement, control, and laboratory use: • IEC 61010-1, EN 61010-1 • UL 3111-1, UL 61010B-1 • CAN/CSA C22.2 No. 1010.1	For UL and other safety certifications, refer to the product label or visit `ni.com`.
Emissions	EN 55011 Class A at 10 m FCC Part 15A above 1 GHz	—
Immunity	EN 61326:1997 + A2:2001, Table 1	—
EMC/EMI	CE, C-Tick, and FCC Part 15 (Class A) Compliant. For EMC compliance, you *must* operate this device with shielded cabling.	—
This product meets the essential requirements of applicable European Directives, as amended for CE marking, as follows:		
Low-Voltage Directive (safety)	73/23/EEC	—
Electromagnetic Compatibility Directive (EMC)	89/336/EEC	—
Note: Refer to the Declaration of Conformity (DoC) for this product for any additional regulatory compliance information. To obtain the DoC for this product, visit `ni.com/hardref.nsf/`.		

Physical

Table 15.

Specification	Value		Comments
Dimensions	Single 3U PXI Slot. CompactPCI compatible.		—
Front Panel Connectors			
Label	Functions	Connector Type	
CH 0	Analog Input	BNC female	
CH 1	Analog Input	BNC female	
TRIG	External Trigger	BNC female	
CLK IN	Sample Clock Input and Reference Clock Input	SMB jack	
CLK OUT	Sample Clock Output and Reference Clock Output	SMB jack	
AUX I/O	PFI 0, PFI 1	9-pin mini-circular DIN	
Front Panel Indicators			
LEDs	Access LED	Active LED	For more information, refer to the *NI High-Speed Digitizers Help*.
	The Access LED indicates the status of the PCI bus and the interface from the NI 5122 to the controller.	The Active LED indicates the status of the onboard acquisition hardware of the NI 5122.	

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